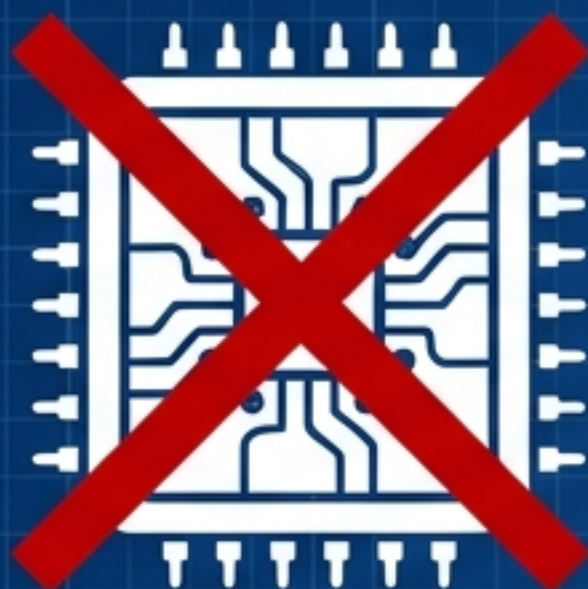




# Defining the Constraints of a Broadly Defined Problem



## The Core Challenge

Strictly discrete electronic components. No PLCs. No microcontrollers.

Automation must be achieved purely through analog circuitry and digital logic.

## Operational Parameters (GA1: Identify)

- Implement stage-by-stage individual testing.
- Analog sensor output between 0V and 1V.
- Amplifier gain strictly capped at  $\leq 5$  (requires multi-stage buffered amplification).

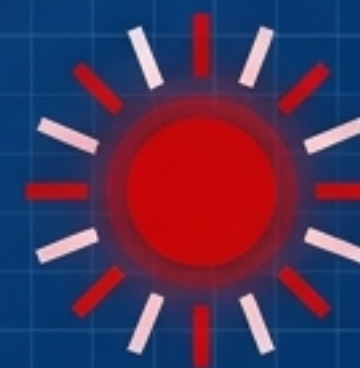
## The System State Success Criteria



Safe Capacity  
(0-11 vehicles)



Filling Capacity  
(12-18 vehicles)

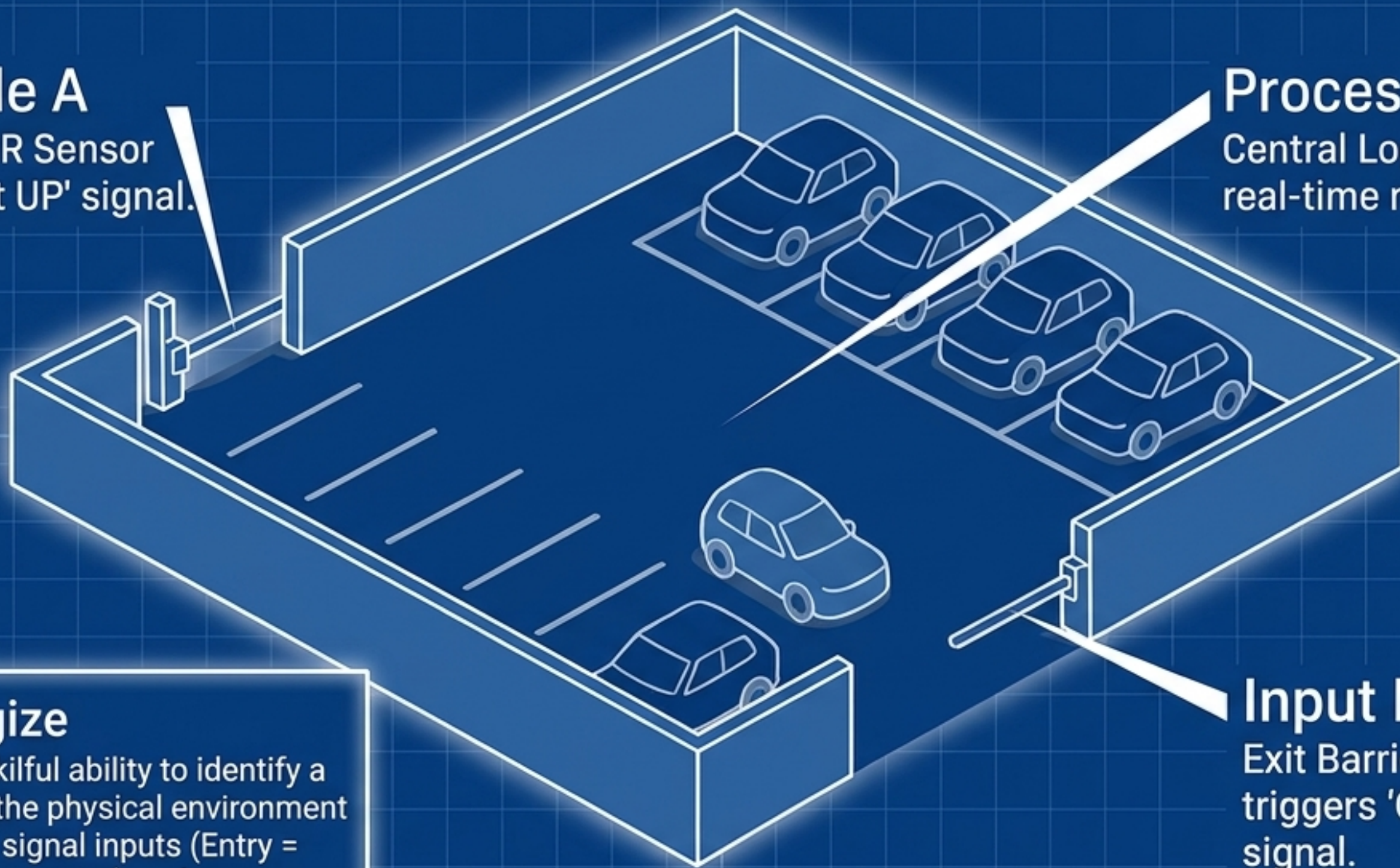


Maximum Capacity Reached  
(Flashing Alert)

# Formulating the Strategy: The Physical Architecture

## Input Node A

Entry Barrier: IR Sensor triggers 'Count UP' signal.



## Processing Node

Central Logic: Calculates real-time net occupancy.




## GA1: Strategize

Demonstrating a skilful ability to identify a strategy: breaking the physical environment down into discrete signal inputs (Entry = Addition, Exit = Subtraction) to drive an automated feedback loop.

## Input Node B

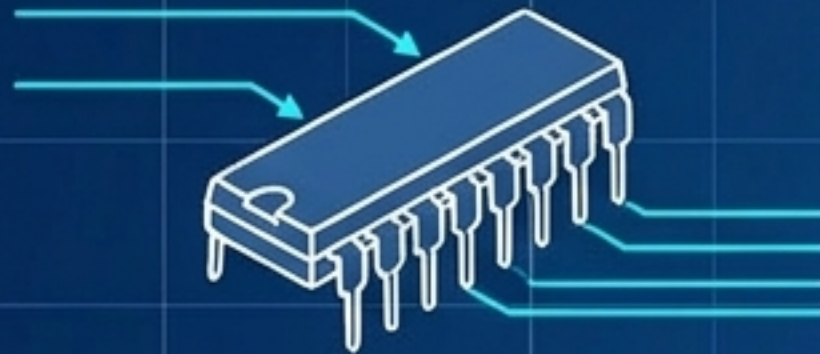
Exit Barrier: IR Sensor triggers 'Count DOWN' signal.

## The System State Matrix

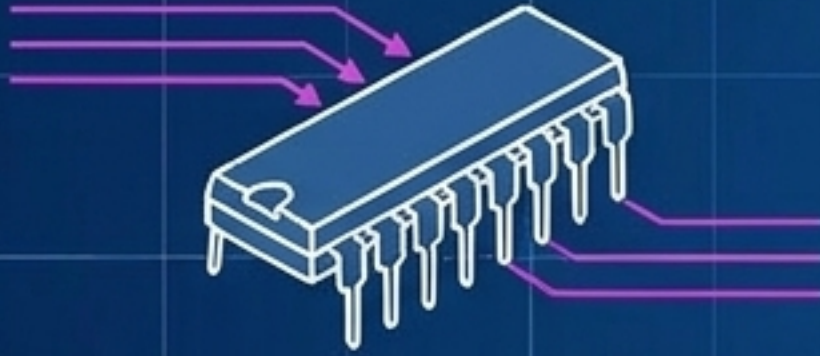
Vehicle Count	Visual Indicator	Logic Condition	Active Sub-Circuit
00 - 11	 Solid Green	$Q < 12$	74LS08 Combinational Logic
12 - 18	 Solid Amber	$12 \leq Q \leq 18$	74LS08 Combinational Logic
19 (Max)	 Flashing Red	$Q \geq 19$	NE555 Timer Triggered

This matrix defines the precise binary conditions that the discrete logic gates must decode. Every physical vehicle translates directly into a binary state.

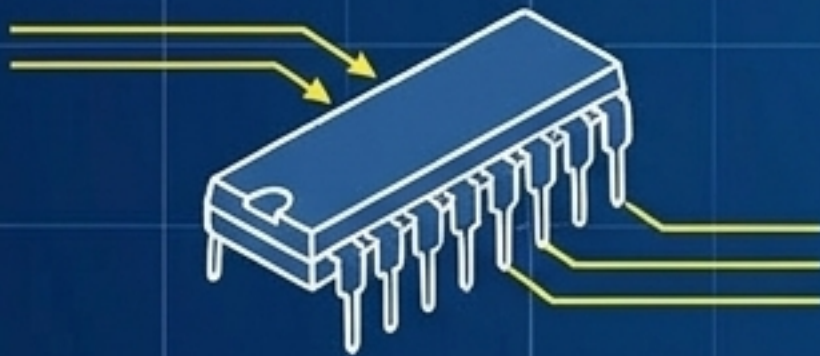
# Component Architecture: Hardware as Software



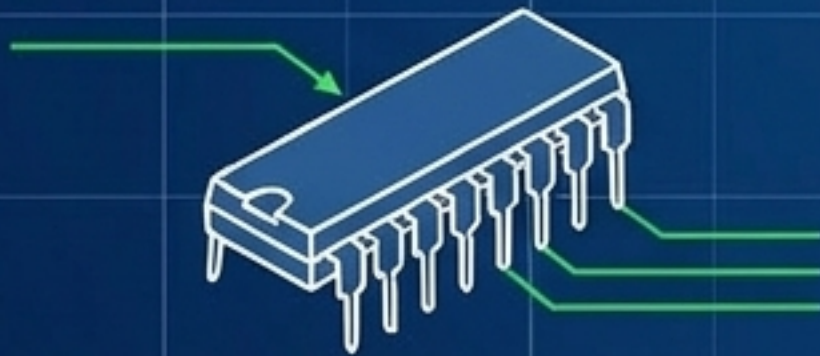
**LM358 (Operational Amplifier)**  
Function: Analog Comparator  
Input: Variable photodiode voltage  
Output: Clean 0V/5V digital pulse



**74LS192 (Decade Counter)**  
Function: Synchronous Up/Down Counting  
Input: Directional pulses  
Output: Binary Coded Decimal (BCD)



**74LS48 (Decoder/Driver)**  
Function: Translation  
Input: BCD from counter  
Output: 7-Segment display matrix

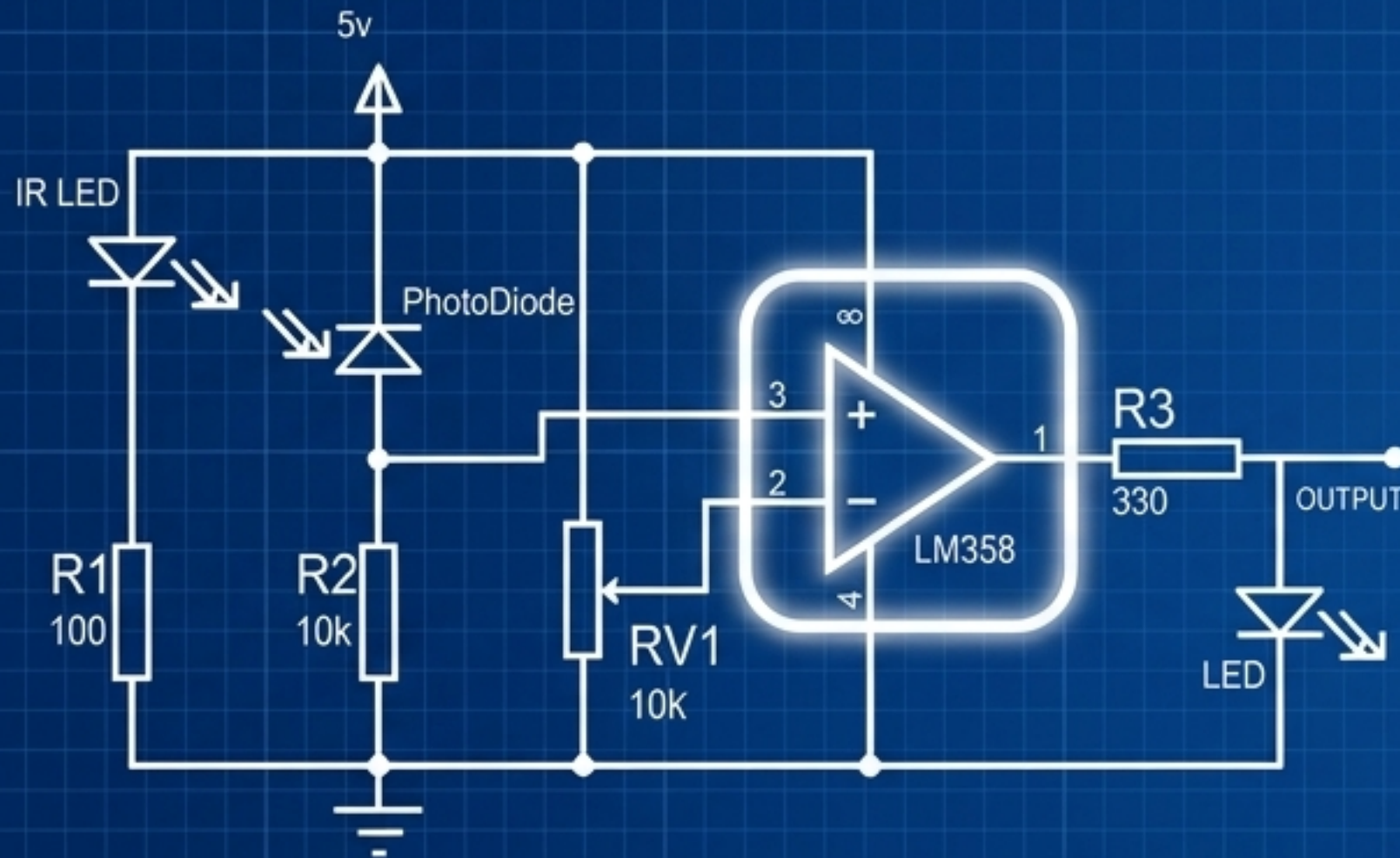


**NE555 (Timer)**  
Function: Astable Multivibrator  
Input: Logic HIGH from Max Capacity limit  
Output: Oscillating flashing alert

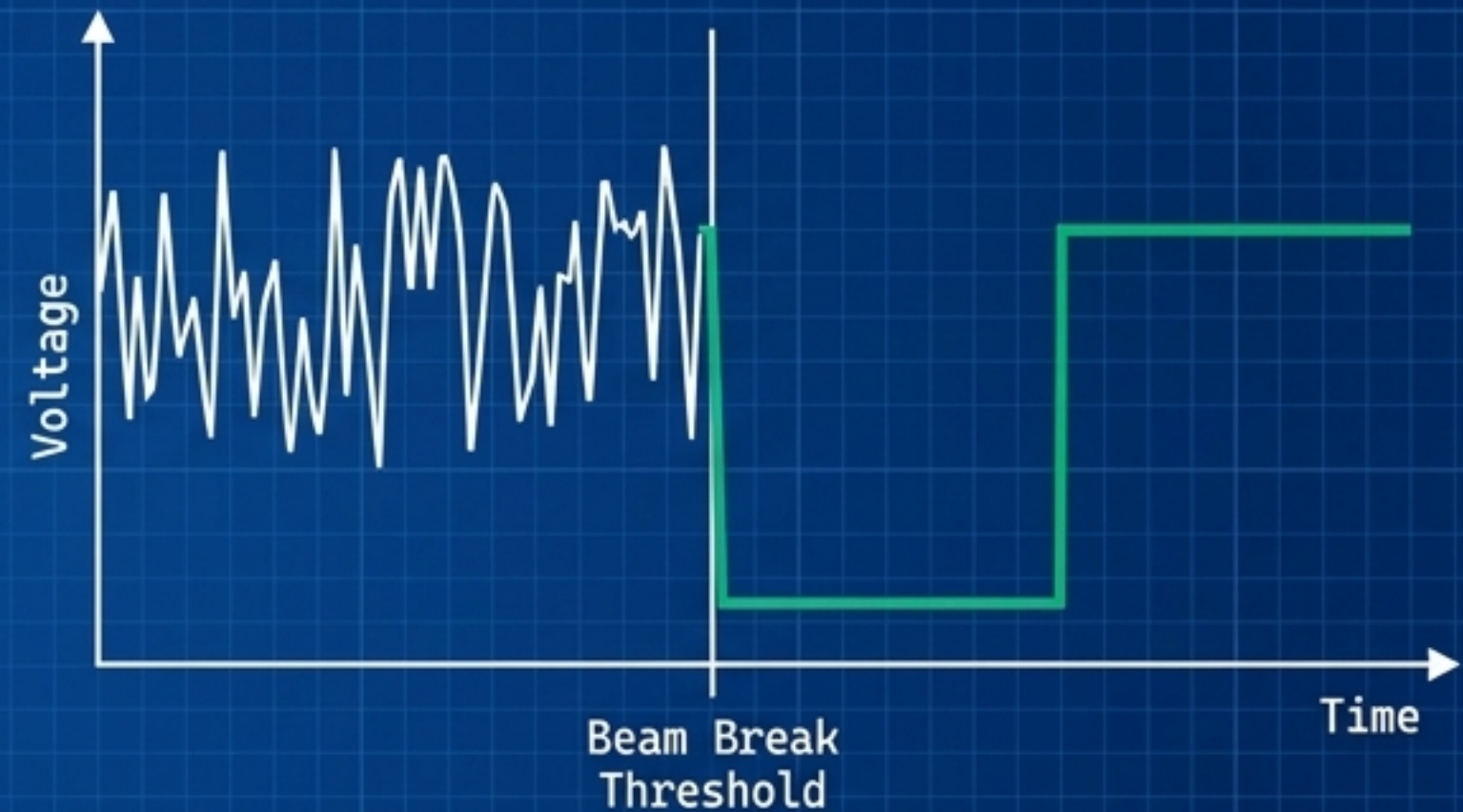
## GA1: Select Solutions

By carefully analyzing and selecting these specific discrete components, we replicate the logical branching of software code (If/Then statements) entirely in hardware.

# Stage 1: The IR Comparator Engine



## The Activation Curve

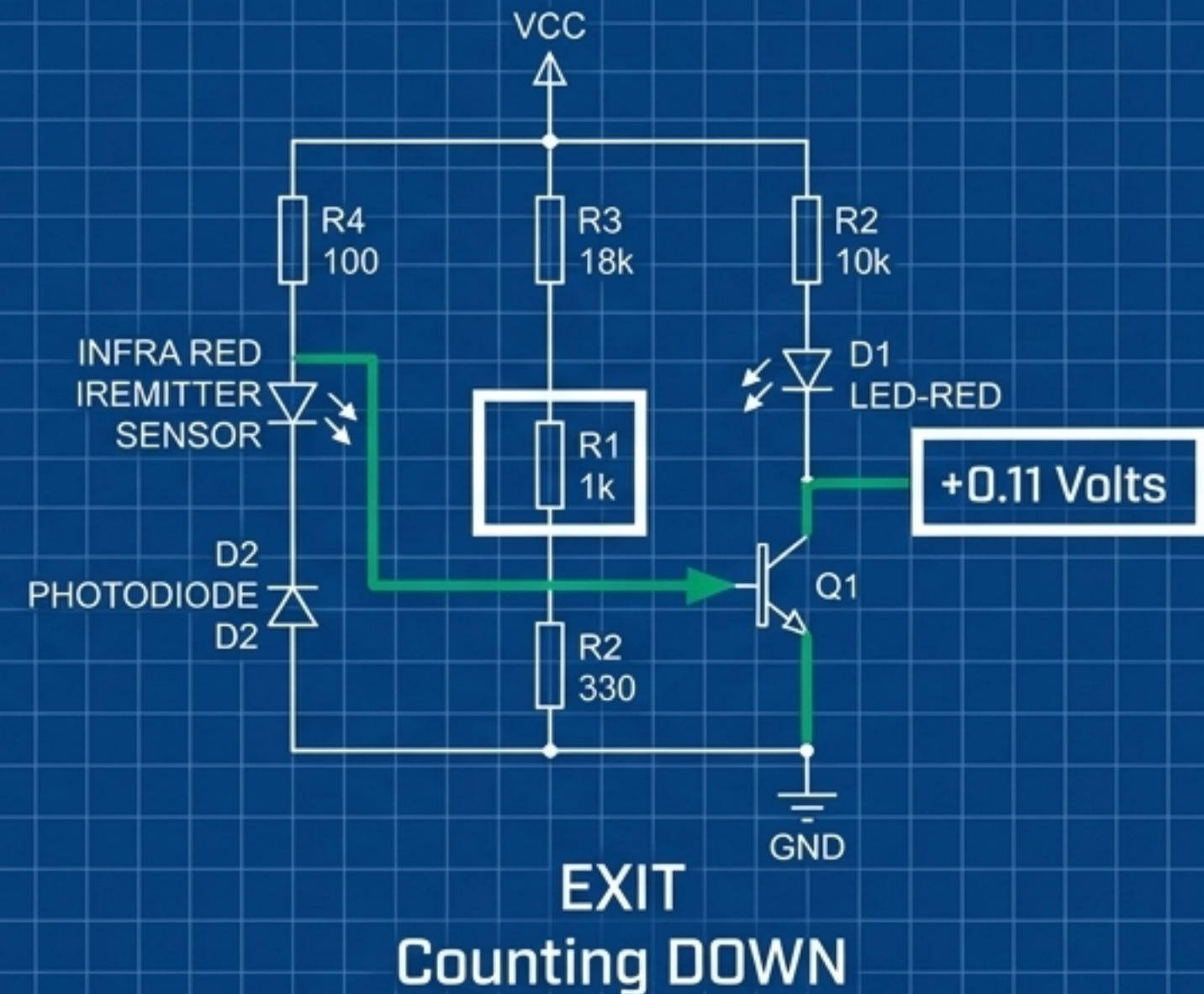
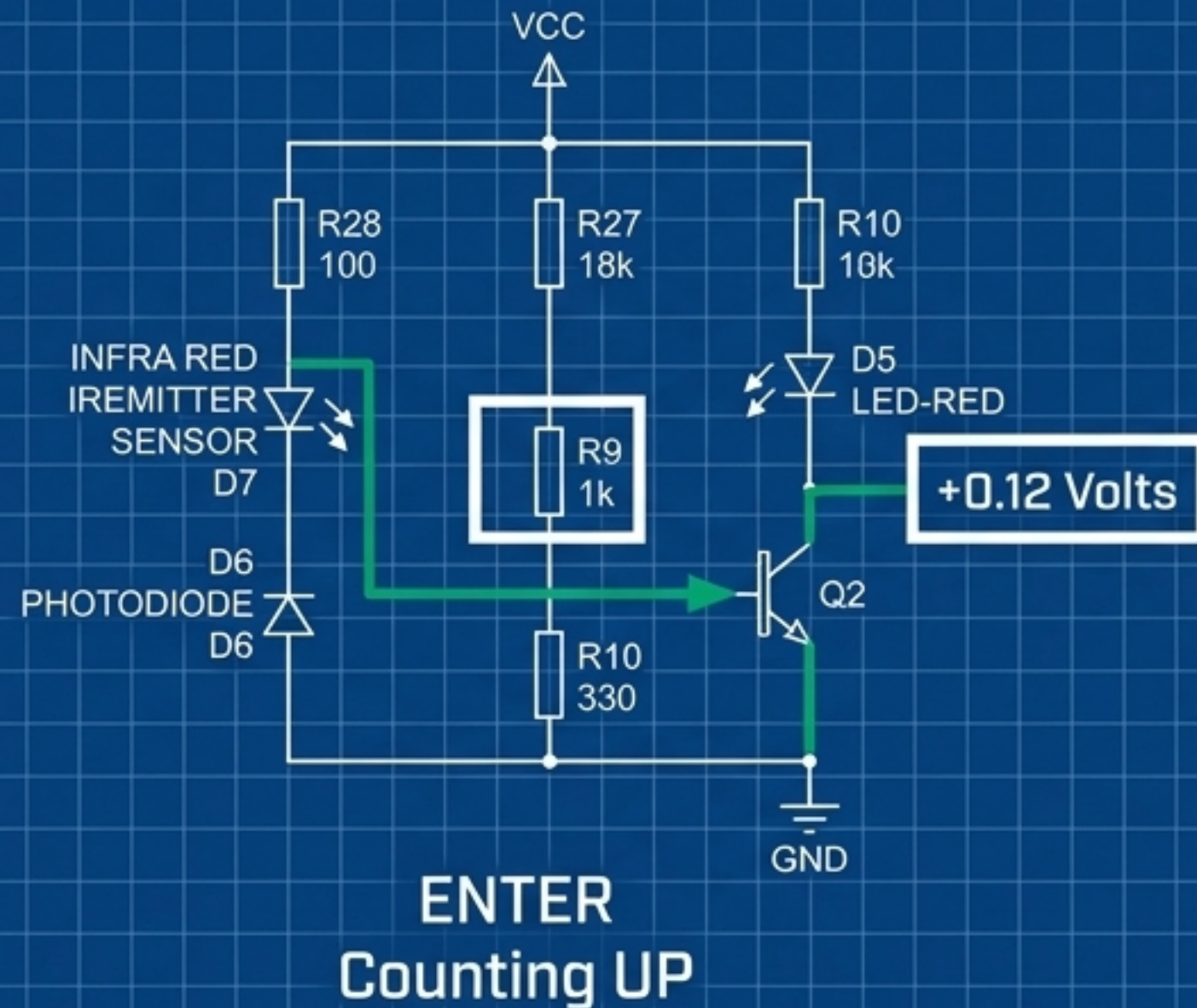


D7 (IR Emitter) maintains constant beam to D6 (Photodiode).

R27 (18k) and R28 (100) dictate baseline analog voltage.

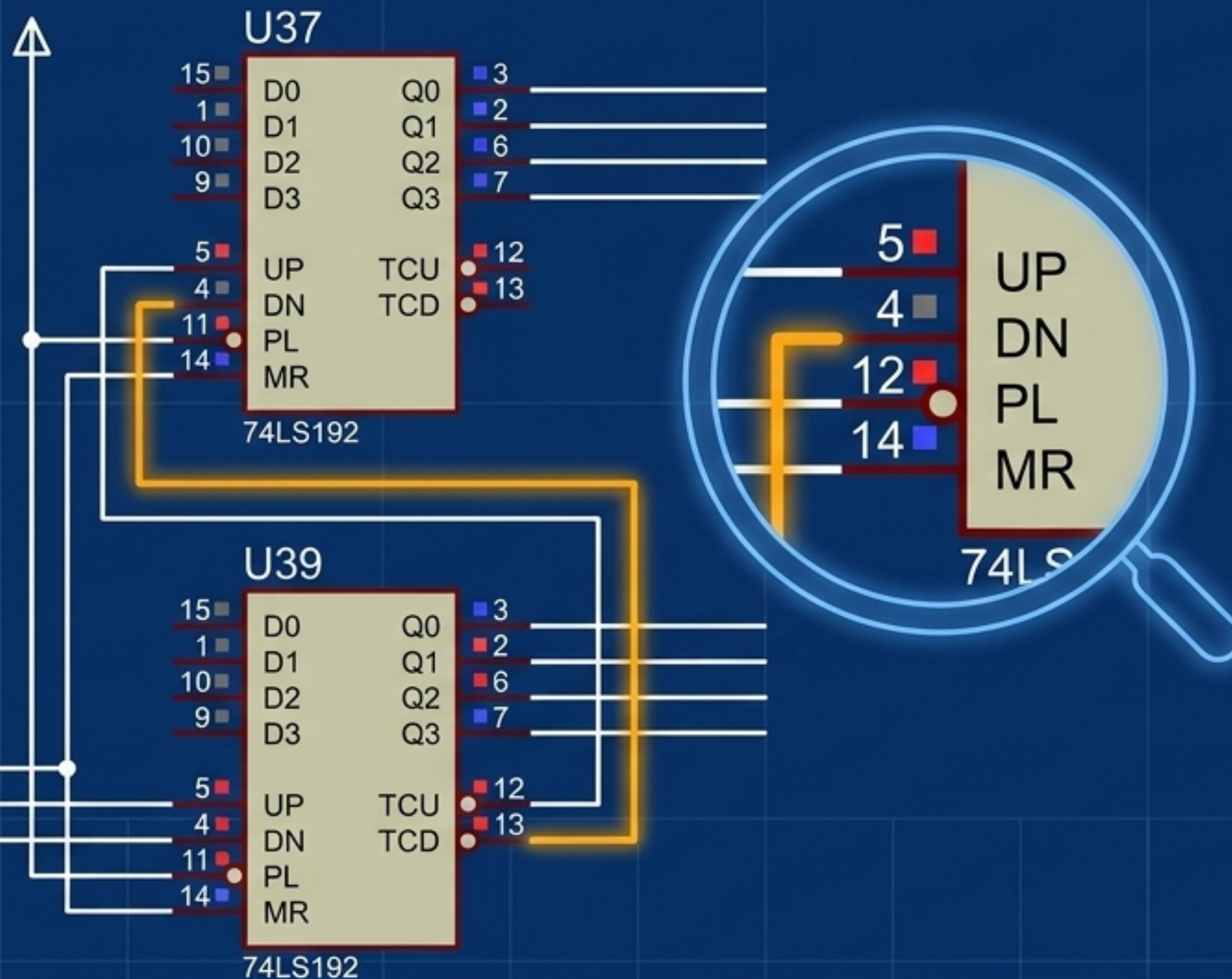
When the beam breaks, the analog voltage shift is instantly digitized by the LM358 comparator, generating a clean count pulse.

# Stage 1B: Pulse Conditioning & Directional Routing



Before reaching the counters, the raw signals are conditioned using NPN transistors (Q1, Q2) to act as clean, isolated switches. This ensures that electrical noise from the external environment does not trigger false counts on the main logic board.

# Stage 2: The Synchronous Cascade Counter



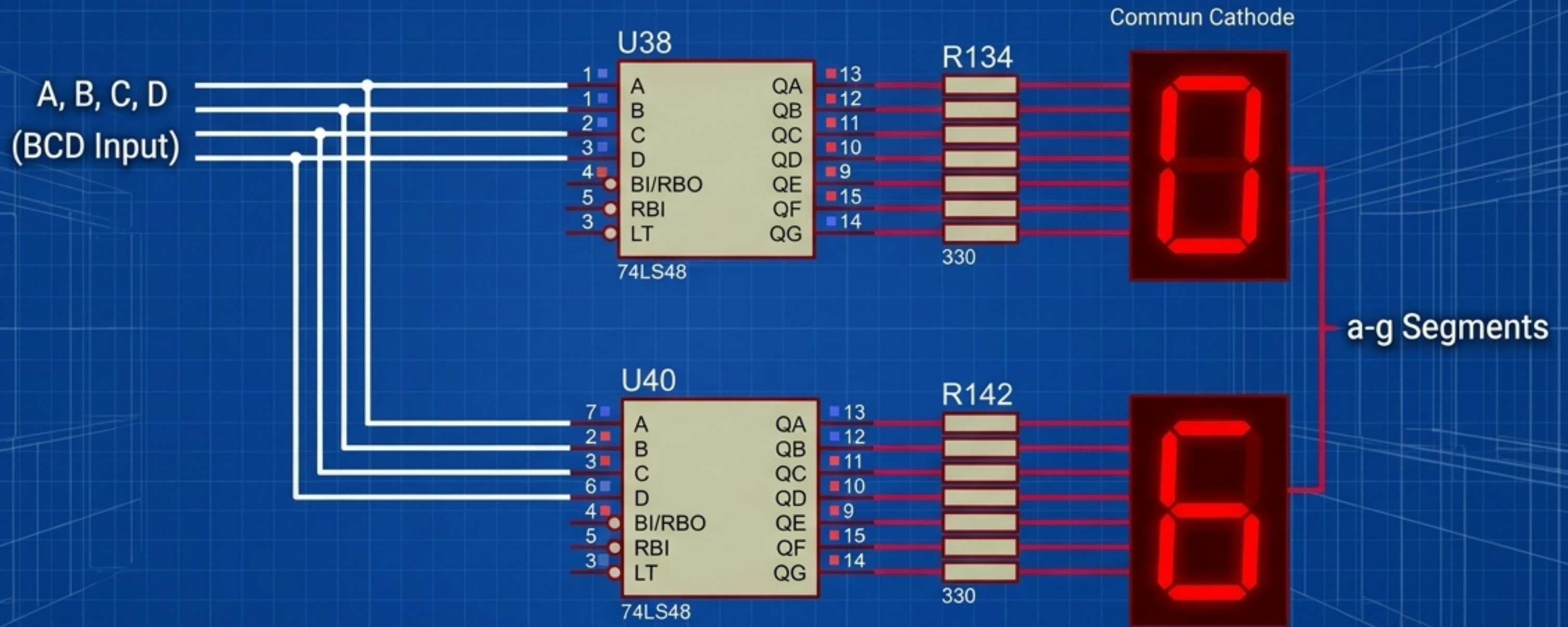
How do we count past 9 without memory?

The U39 IC handles the "Units" column. When it overflows from 9 to 0, Pin 12 (TCU) emits a "Carry" pulse.

This single pulse triggers U37 (the "Tens" column) to step up by exactly one.

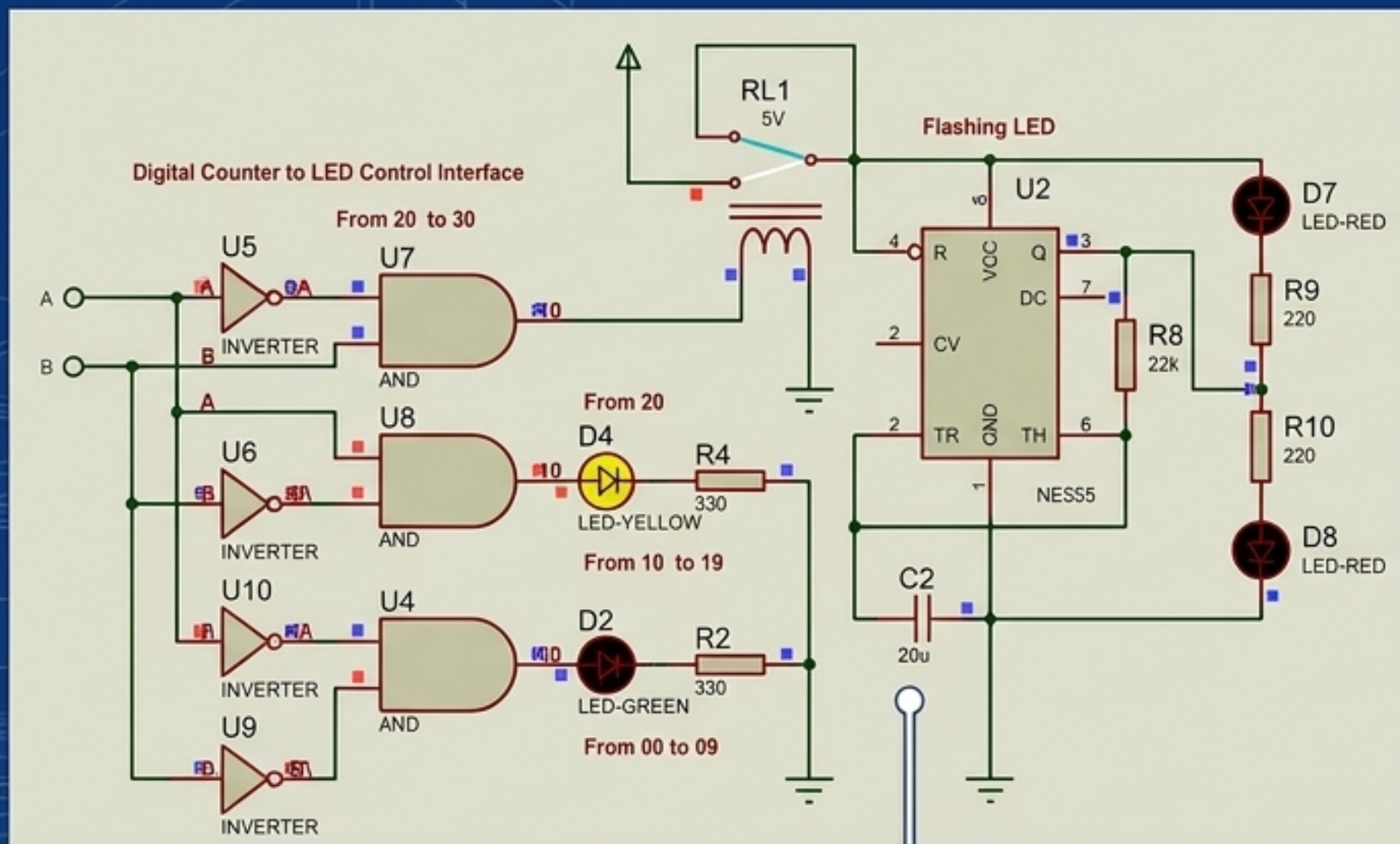
This hardware cascade creates infinite scalability without a single line of code.

# Stage 3: Decoding Binary to Human-Readable Output



The 74LS48 acts as a hardware translator. It constantly reads the 4-bit Binary Coded Decimal (BCD) from the counters and maps it to the specific pinout required to illuminate the Common Cathode 7-segment displays. The 330Ω resistors ensure current limitations, protecting the LEDs from thermal runaway.

# Stage 4: Automated State Monitoring & Alert



Condition Met:



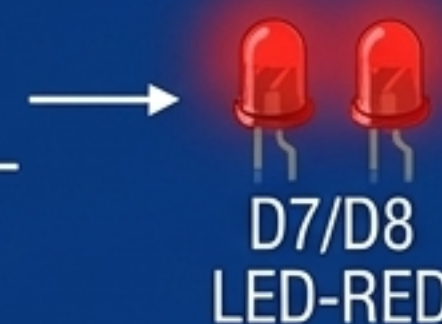
Gate Logic:

Inverters and AND gates output a HIGH signal only when the exact binary string for maximum capacity is present.

Trigger:

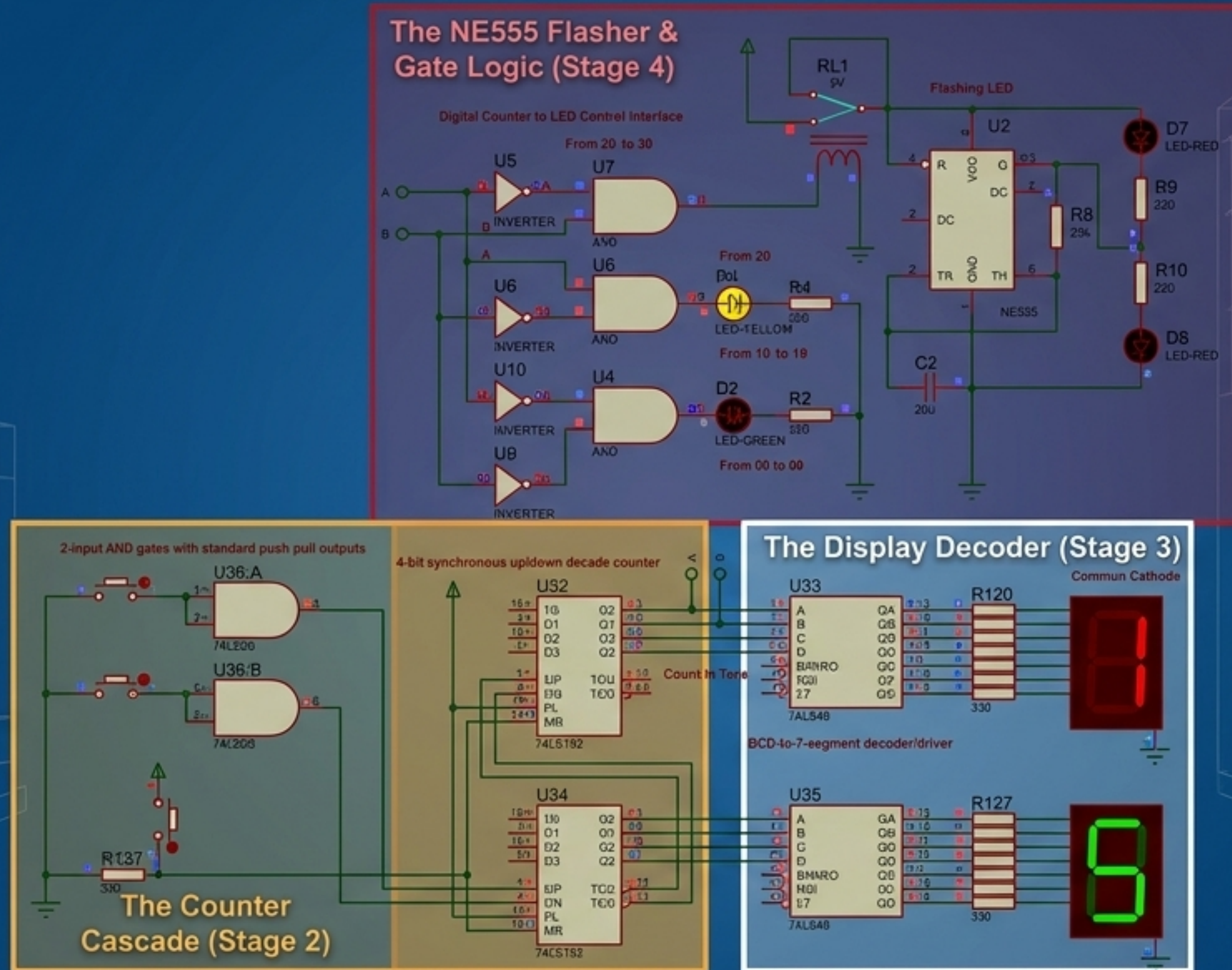
This HIGH signal routes to Pin 4 (Reset) of the NE555 timer.


Output:



**Pure hardware state detection:** The NE555 astable multivibrator remains dormant until the exact binary conditions of maximum capacity unblock its reset pin.

# Full System Integration (GA1: Implement Practical Solution)



A fully realized automated system. Analog sensors trigger digital logic, counters iterate, decoders translate, and combinational gates monitor thresholds—all shaking hands simultaneously in a perfectly closed feedback 

# Bridging Hardware and Software



**Engineer:** Henock HNK

**Philosophy:** Technology should solve real problems. The best solutions emerge from curiosity, persistence, and mastering the fundamentals across both analog electronics and modern software stacks.

**Core Competencies Demonstrated:**

- Circuit Design
- Digital Electronics
- Embedded Systems Logic
- Systems Engineering

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From discrete logic parkades to cloud-connected IoT arrays—turning complex constraints into working systems.

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